THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte WALTER E. GIBSON

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Appeal No. 1997-3132
Application 08/268,370[1]

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ON BRIEF

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Before HAIRSTON, FLEMING and LALL, ***Administrative Patent Judges***.

FLEMING, ***Administrative Patent Judge***.

DECISION ON APPEAL

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[1] Application for patent filed June 30, 1994.

This is a decision on appeal from the final rejection of claims 2 through 5 and 8, all the claims pending in the application. Claims 1, 6 and 7 have been cancelled.

The invention relates to using scan test techniques to test the interconnecting signal lines between digital circuits employing different or non-compatible scan test architectures.

Independent claim 8 is reproduced as follows:

8. A method of testing an interconnect that couples first and second digital circuits to one another for communicating data signals therebetween, the first digital circuit being structured to include a scan architecture specified by IEEE Standard 1149.1 that includes a first number of scannable data registers, the second digital circuit employing a scan archi- tecture different from that of the first digital circuit that includes a second number of data registers, the first and second numbers of scannable data registers being coupled to the inter- connect for applying data signals thereto and to receive data signals therefrom, the method including the steps of:

(a) applying a first test pattern to the second number of scannable data registers;

(b) sampling the interconnect with the first number of scannable data registers according to a protocol required by the IEEE Standard 1149.1 that includes the steps of,

(i) capturing data signals of the interconnect by the first number of scannable data registers,

(ii) shifting into the first number of scannable data registers a second test pattern,

(iii) again capturing data signals of the interconnect by the first number of scannable data registers, and

(iv) shifting the captured data signals from the first number of scannable data registers;

(c) sampling data signals on the interconnect by the second number of scannable data registers;

(d) shifting the sampled data signals from the second number of scannable data registers; and

(e) comparing the captured data signals and the sampled data signals to first and second standard patterns, respectively, to determine the integrity of the interconnect; and

(f) repeating steps (a) - (e) for a plurality of additional test patterns.

The Examiner relies on the following references:

Farwell	5,202,625	Apr. 13, 1993
Shiono et al. (Shiono) (effective filing dates: Jan. 31 and May 28, 1992)	5,390,191	Feb. 14, 1995
Gruetzner et al. (Gruetzner) (effective filing date: July 17, 1992)	5,444,715	Aug. 22, 1995

Claims 8 and 3 through 5 stand rejected under 35 U.S.C. § 103 as being unpatentable over Shiono in view of Gruetzner. Claim 2 stands rejected under 35 U.S.C. § 103 as being unpatentable over Shiono in view of Gruetzner and Farwell.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the briefs[2] and answers[3] for the respective details thereof.

OPINION

We will not sustain the rejection of claims 2 through 5 and 8 under 35 U.S.C. § 103.

The Examiner has failed to set forth a ***prima facie*** case. It is the burden of the Examiner to establish why one

[2] Appellant filed an appeal brief on August 22, 1996. Appellant filed a reply brief on December 30, 1996. The Examiner responded to the reply brief with a supplemental Examiner's answer, thereby entering the reply brief into the record.

[3] The Examiner filed an Examiner's answer on October 28, 1996. In response to the reply brief, the Examiner filed a supplemental Examiner's answer on March 23, 1997.

having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior art, or by implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordnance Mfg. v. SGS Importers Int'l, Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied***, 519 U.S. 822 (1996) ***citing W. L. Gore & Assoc., Inc. v. Garlock, Inc.***, 721 F.2d 1540, 1548, 220 USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied,*** 469 U.S. 851 (1984).

Appellant argues on pages 5 through 7 of the brief and in the reply brief that neither Shiono nor Gruetzner teaches or suggests a method of testing an interconnect that couples first and second digital circuits in which the first digital circuit

employs a scan architecture specified by the IEEE Standard 1149.1 and the second digital circuit employs a scan architecture different from that of the first digital circuit. Appellant points out that neither Shiono nor Gruetzner teaches or suggests the concept of testing an interconnect with incompatible scan architectures. In particular, Appellant points out on pages 5 and 6 that Shiono teaches testing an interconnect using two circuits that are the same and therefore of compatible scan architectures. Appellant further points out on page 6 that Gruetzner teaches that the scan architecture used by the two circuits are the same and therefore compatible. Appellant states that the references are absent of any teaching of Appellant's novel feature of the invention of claim 8, which is the method used to check the interconnect between the first and second digital circuits where the first digital circuit employs a scan architecture specified by the IEEE Standard 1149.1 and the second digital circuit employs a scan architecture that is different from that of the first.

On page 4 of the Examiner's answer, the Examiner acknowledges that Shiono does not teach or disclose that the second digital circuit employs a scan architecture that is different from that of the first digital circuit. Furthermore,

the Examiner does not show that Gruetzner teaches that the scan architecture of the second digital circuit is different than that of the first digital circuit. The Examiner states that it would be obvious for one of ordinary skill in the art at the time to change the scan architecture of the second digital circuit in Shiono because Gruetzner teaches that their invention is particularly beneficial in a boundary-scan architecture and points to column 4, lines 1-5. The Examiner further emphasizes this point on page 3 of the supplemental Examiner's answer. There, the Examiner states that Gruetzner teaches in column 3, line 67, through column 4, line 5, that the invention is particularly beneficial in boundary-scan architecture and thus provides motivation to one of ordinary

skill in the art to form in Shiono an architecture that includes incompatible scan architecture as claimed.

Upon our detailed review of Gruetzner, we fail to find that Gruetzner suggests incompatible architecture or, for that matter, recognizes the problem of incompatible architectures and how to test the interconnect between them. In column 3, line 67, through column 4, line 5, Gruetzner simply states that the invention may be used in other than level sensitive scan designs. Gruetzner is not suggesting that the invention would be used in

scan designs that are incompatible, only that it is possible to use it in other compatible sensitive scan designs.

The Federal Circuit states that "[t]he mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." ***In re Fritch***, 972 F.2d 1260, 1266 n.14, 23 USPQ2d 1780, 1783-84

n.14 (Fed. Cir. 1992), ***citing In re Gordon***, 733 F.2d 900, 902, 221 USPQ 1125, 1127 (Fed. Cir. 1984).

We fail to find that Shiono or Gruetzner provides any reason or suggestion of the desirability of the modification proposed by the Examiner. Therefore, we will not sustain the Examiner's rejection of claims 3 through 5 and 8 under 35 U.S.C. § 103 as being unpatentable over Shiono in view of Gruetzner.

Claim 2 stands rejected under 35 U.S.C. § 103 as being unpatentable over Shiono in view of Gruetzner and Farwell. We note that the Examiner relies on the above same reasoning for modifying Shiono to provide an incompatible scan architecture for the second circuit. We fail to find that Farwell supplies the missing teaching or suggestion to those skilled in the art to make the modification as proposed by the Examiner. Therefore, we will not sustain the Examiner's rejection of claim 2 for the same reasons as above.

In view of the foregoing, the decision of the Examiner rejecting claims 2 through 5 and 8 is reversed.

REVERSED

KENNETH W. HAIRSTON)
Administrative Patent Judge)
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) BOARD OF PATENT
MICHAEL R. FLEMING) APPEALS AND INTERFERENCES
Administrative Patent Judge)
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PARSHOTAM S. LALL)
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